# SuperVidel

## **Memory Map**

Rev 7 2016-07-13

## History

Date	Version	Changed
12-03-12	1	Initial release
12-09-18	2	Changed Blit mode "0111" to (Src1.alpha*alpha_reg) from just alpha_reg.
12-09-23	3	Added Replacement RGB values in blitter reg 0x80010078.
13-01-19	4	Added firmware revision register at 0x8001007C.
13-08-18	5	Added new function of Done INT flag in reg 0x80010078.
15-12-06	6	Added Sblitter FIFO write port and status flags
16-07-13	7	Ethernet MAC core data buffers are removed from FW v010

#### DDR2 RAM

Address	Size	Access types	Description
0xA0000000	16MB	-	Shadow of ST-RAM in DDR2 SDRAM
0xA1000000	112MB	Byte/ Word/ Long Re+Wr	DDR2 SDRAM general purpose graphics RAM

#### Super Videl settings registers

Address	Size	Access types				D	escript	ion			
0x80010000	Long	Long	Gene	eral pu	irpose	settin	gs/sta	atus re	egister	,	
			Bit				31	:24			
			Name				Res	erved			
			Read/ Write				I	R			
			Reset value				%000	00000			
			Bit	23	22	21	20	19	18	17	16
			Name	Reserv ed	DVI VSYNC int flag	DVI VSYNC int en	VGA VSYNC int flag	VGA VSYNC int en	HW revision	DVI protect	VGA protect
			Read/ Write	R	R+W	R+W	R+W	R+W	R	R+W	R+W
			Reset value	0	0	0	0	0	?	0	0
			Bit	15	14	13	12	11	10	9	:8
			Name	DVI clk is from clock chip	DVI videl clk is 25.175 MHz	VGA clk is from clock chip	VGA videl clk is 25.175 MHz	Videl 25.175 MHz valid	Videl 32MHz valid	Monite	or type
			Read/ Write	R	R	R	R	R	R	R	١W
			Reset value	?	?	?	?	?	?	%	10
			Bit	7	6	5	4	3	2	1	0
			Name	DVI connect ed	SV mode	DVI Hsync	DVI Vsync	VGA Hsync	VGA Vsync	DVI reset	VGA reset
			Read/ Write	R	R	R	R	R	R	R+W	R+W
			Reset value	0	1	?	?	?	?	1	1
				'1' to ho	old VGA VGA ou		ystem lo	ogic in r	eset. No	screen	is

			]
DVI rese			
	to hold DVI video system	n logic in	reset. No screen is
	n the DVI output.		
	nc active:		
	ly status bit. Is '1' when a	Vsync is	s in progress on VGA
output.			
	ync active:		
	ly status bit. Is '1' when a	Hsync i	s in progress on VGA
output.			
	nc active:		
	ly status bit. Is '1' when a	Vsync is	s in progress on DVI
output.			
	nc active:		
	ly status bit. Is '1' when a	Hsync i	s in progress on DVI
output.			
SV mode			
	ly status bit. Is '1' when the		
	lel register mode, i.e. the		
	to be written, and the re		5
	lel registers. If the Videl r		
	he resolution output is de		
	'0'. A copy of this bit can		
			e user program reads out
	registers before changin	•	
			ores the old Videl register
	the status of this bit will b		
		ne ola Su	perVidel resolution or the
	resolution.		
DVI conr			ad to the DV/Lineart 101
	wered-on DVI monitor is	connect	ed to the DVI port. "O"
otherwise			
Monitor	type:	ly for the	Widel compatiblity. The
Monitor Fake mo	type: nitor type setting used or		
Monitor Fake mon actual co	type: nitor type setting used or nnected monitor type is I	NOT dete	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or	NOT dete	ected by the hardware.
Monitor Fake mon actual co	<b>type:</b> nitor type setting used or onnected monitor type is I itor type only applies to t	NOT dete he analo	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type	NOT dete he analo Value	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type Monochrome	NOT dete he analo Value	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type	NOT detended he analo Value ″00″ ″01″	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type Monochrome	NOT dete he analo Value	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type Monochrome RGB - Colormonitor	NOT detended he analo Value ″00″ ″01″	ected by the hardware.
Monitor Fake mon actual co	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type Monochrome RGB - Colormonitor VGA - Colormonitor	NOT detended he analo Value "00" "01" "10"	ected by the hardware.
Monitor Fake mon actual co The mon	type: nitor type setting used or onnected monitor type is I itor type only applies to t Monitor type Monochrome RGB - Colormonitor VGA - Colormonitor	NOT detended he analo Value "00" "01" "10"	ected by the hardware.
Videl 321	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV	NOT dete he analo <b>Value</b> "00" "01" "10" "11"	ected by the hardware.
Videl 321 Says if th CT60) is	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But	VOT dete he analo Value ″00″ ″01″ ″10″ ″11″ m the fal	ected by the hardware. g (VGA) output. Values:
Videl 321 Says if th CT60) is	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from	VOT dete he analo Value ″00″ ″01″ ″10″ ″11″ m the fal	ected by the hardware. g (VGA) output. Values:
Videl 321 Says if th CT60) is Videl 25.	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But	VOT dete he analo "00" "01" "10" "11" m the fal	con motherboard (or from s the correct frequency.
Videl 321 Says if th CT60) is Videl 25. Says if th	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But .175MHz valid:	VOT dete he analo <b>Value</b> "00" "01" "10" "11" m the fal t not if it k from th	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is
Videl 321 Says if th CT60) is Videl 25. Says if th detected	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But .175MHz valid: ne input 25.175 Mhz clock	VOT dete he analo <b>Value</b> "00" "01" "10" "11" m the fal t not if it k from th	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is
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Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clocel as running. But not if it is el clk is 25.175MHz:	VOT dete he analo Value "00" "01" "10" "11" m the fal not if it i s from th s the corr ock is ch	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency.
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Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monitor type Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz cloccl as running. But not if it is lel clk is 25.175MHz: ne Videl 25.175MHz(1) cl o) for VGA clock selection	VOT dete he analo <b>Value</b> "00" "01" "10" "11" m the fal not if it it the corr ock is ch MUX.	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency.
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monitor type Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clocd as running. But not if it is lel clk is 25.175MHz: ne Videl 25.175MHz(1) cl 0) for VGA clock selection is from clock chip:	VOT dete he analo <b>Value</b> "00" "01" "10" "11" m the fal not if it it the corr ock is ch MUX.	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency.
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA videl 25.	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clock as running. But not if it is lel clk is 25.175MHz(1) cl 0) for VGA clock selection is from clock chip: A clock net is driven by the	VOT dete he analo <b>Value</b> "00" "01" "10" "11" m the fal not if it it the corr ock is ch MUX.	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency.
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA videl 25. DVI Vide	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But .175MHz valid: ne input 25.175 Mhz clock as running. But not if it is lel clk is 25.175MHz(1) cl 0) for VGA clock selection is from clock chip: A clock net is driven by the 175 or 32MHz clock (0). el clk is 25.175MHz:	VOT dete he analo <b>Value</b> "00" "10" "11" m the fal not if it it s the corr ock is ch ock is ch MUX. e CDCE	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency. losen instead of the 925 clock chip(1), not a
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA videl 25. DVI Vide Says if th	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clock as running. But not if it is lel clk is 25.175MHz(1) cl b) for VGA clock selection is from clock chip: A clock net is driven by the 175 or 32MHz clock (0). El clk is 25.175MHz: ne Videl 25.175MHz: he Videl 25.175MHz(1) cl	VOT dete he analo Value "00" "01" "10" "11" m the fal not if it i k from th s the corr ock is ch MUX. e CDCEs	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency. losen instead of the 925 clock chip(1), not a
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA videl 25. DVI Vide Says if th 32MHz(0	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clocel as running. But not if it is sel clk is 25.175MHz(1) cl 0) for VGA clock selection is from clock chip: A clock net is driven by the 175 or 32MHz clock (0). El clk is 25.175MHz(1) cl 175MHz(1) cl 17	VOT dete he analo Value "00" "01" "10" "11" m the fal not if it i k from th s the corr ock is ch MUX. e CDCEs	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency. losen instead of the 925 clock chip(1), not a
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA videl 25.1	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clocel as running. But not if it is lel clk is 25.175MHz(1) cl 0) for VGA clock selection is from clock chip: A clock net is driven by the 175 or 32MHz clock (0). I clk is 25.175MHz(1) cl 0) for DVI clock selection s from clock chip: Note: the time time time time time time time tim	VOT dete he analo Value "00" "11" "11" m the fal not if it i k from th s the corr ock is ch MUX. e CDCES	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency. losen instead of the 925 clock chip(1), not a losen instead of the
Videl 321 Says if th CT60) is Videl 25. Says if th detected VGA Vid Says if th 32MHz(0 VGA clk The VGA videl 25. DVI Vide Says if th 32MHz(0 DVI clk is The DVI	type: nitor type setting used or onnected monitor type is I itor type only applies to the Monochrome RGB - Colormonitor VGA - Colormonitor TV MHz valid: ne input 32 Mhz clock from detected as running. But 175MHz valid: ne input 25.175 Mhz clocel as running. But not if it is sel clk is 25.175MHz(1) cl 0) for VGA clock selection is from clock chip: A clock net is driven by the 175 or 32MHz clock (0). El clk is 25.175MHz(1) cl 175MHz(1) cl 17	VOT dete he analo Value "00" "11" "11" m the fal not if it i k from th s the corr ock is ch MUX. e CDCES	ected by the hardware. g (VGA) output. Values: con motherboard (or from s the correct frequency. e falcon motherboard is rect frequency. losen instead of the 925 clock chip(1), not a losen instead of the

			VGA protect: If 1 it will protessettings when Videl resolution <b>DVI protect:</b> If 1 it will protessettings when Videl resolution <b>HW revision:</b> Is 1 if the SV I <b>VGA/DVI VBI</b> Writing VGA of VGA or DVI go INT flag will bo 0 to the right I vector numbe 0x320) (for DV	ect the VGA o Videl registe on will appear ect the DVI ou Videl registe on will appear hardware is a <b>INT enable</b> or DVI INT ena enerate an in e set to 1. You Done INT flag r 0xC7 (addre	rs are written. on VGA. utput from swi rs are written. on DVI. revision 1. Is <b>&amp; Done INT f</b> able to 1 make terrupt reques u must clear it . Make sure ess 0x31C) (fo	On reset this tching to Vide On reset this 0 for a revision flags es the vertica st, and VGA o t in your hand you put your I or VGA) or 0xt	is 0, so the I register is 0, so the on 2. I sync for r DVI Done ler by writing SR pointer in				
0x80010004	Long	Long Wr only	CDCE925	PLL1-reg1	(DDR clocl	k)					
			Bit	31:24	23:16	15:8	7:0				
			Name	Reg0x17	Reg0x18	Reg0x19	Reg0x1A				
			Read/Write	R+W	R+W	R+W	R+W				
			Reset value	0x01	0x06	0x90	0x13				
0x80010008	Long	Long Wr only	ClockFinder p	•	(DDR cloci						
			Bit		31:8		7:0				
			Name		Reserved		Reg0x1B				
			Read/Write Reset value		R 0x000000		R+W 0x47				
0x8001000C	Long	Long	Use addr 0x11 program. Writ automatically.	e this register	last when se	tting PLL1, to	ockfinder begin update				
		Wr only				-					
			Bit	31:24	23:16	15:8	7:0				
			Name	Reg0x27	Reg0x28	Reg0x29	Reg0x2A				
			Read/Write	R+W	R+W	R+W	R+W				
			Reset value Use addr 0x2 <sup>°</sup> ClockFinder p								
0x80010010	Long	Long Wr only	CDCE925 PLL2-reg2 (Video clock)								
			Bit 31:8 7:0								
			Name		Reserved		Reg0x2B				
			Read/Write		R		R+W				
			Reset value		0x000000		0x00				

				ite this		utput from the 0 r last when set		Clockfinder to begin update		
0x80010014	Long	Long Re+Wr	VGA Scree	en ad	dress	5				
			Bit	31	1:27		26:1	0		
			Name	Res	erved	Video address 0				
			Read/Write	Read/Write R			R+W	R		
			Reset value	00000000 0						
				When	readin	g this add 0xA0		an odd adress is DDR2 base		
0x80010018	Long	Long Re+Wr	VGA Horisontal data begin/end register							
			Bit 31:27 26:16 15:11 10:0							
			Name         Reserved         Hor. data begin         Reserved         Hor. data end							
			Read/Write         R         R+W         R         R+W							
			Reset value	0b000	0b00000	0b0000000000				
0x8001001C	Long	Long Re+Wr		ideo cl	ock pul			ndow ends. value by 2 after		
			Bit	31	30:27	26:16	15:11	10:0		
				Polarity	Reserve		n Reserved			
			Read/Write	R+W	R	R+W	R	R+W		
			Reset value10b00000b00000000000b000000b00000000000000000000000000000000000							
0x80010020	Long	Long Re+Wr	VGA Verti	cal da	ata be	gin/end reg	ister			
			Bit	31:	27	26:16	15:11	10:0		
			Name	Rese	rved	Vert data begin	Reserved	Vert data end		
			Read/Write	R		R+W	R	R+W		
			Reset value	0b00	000	06000000000000000	0b00000	060000000000000000000000000000000000000		
			Vertical data Vertical posit Vertical data	ion (in		es) where the	data windo	ow begins.		

			Vertiour poo		scariines	s) where the			
0x80010024	Long	Long Re+Wr	VGA Vert	ical sy	nc reg	ister			
			Bit	31	30:27	26:16	15:	11	10:0
			Name	Polarity	Reserved	Vert. sync beg	gin Rese	ved Ve	t. sync end
			Read/Write	R+W	R	R+W	R		R+W
			Reset value	1	0b0000	060000000000000000000000000000000000000	00 0b00	000 0b0	000000000000000000000000000000000000000
			Vertical syn Vertical pos Vertical syn Vertical pos	nc begin ition (in s nc end: ition (in s	n: scanlines scanlines	ns sync puls s) where the s) where the	vsync pu vsync pu	ulse beg ulse end	S.
0x80010028	Long	Long Re+Wr	VGA Last	t horis	ontal/v	ertical po	sition r	egiste	r
			Bit	31:2	7	26:16	15:11		10:0
			Name	Reserv	ved La	st hor. pos.	Reserved	Last v	ertical pos.
			Read/Write	R		R+W	R		R+W
			Reset value	0b000	00 0b0	0000000000	0b00000	0b000	00000000
			by 2 after c Last vertica The last ver	alculati al positi tical pos	on. on: sition (in l	efore return ines), i.e. the	0	Divide 1	
0x8001002C	Long	Long Re+Wr	by 2 after c Last vertica	alculati al positi tical pos ches bef	on. on: sition (in l fore retur	ines), i.e. th ning to 0.	0	Divide 1	he value
0x8001002C	Long	-	by 2 after of Last vertica The last ver counter read	alculati al positi tical pos ches bef a amou 31:30	on. on: iition (in l fore retur int regi	ines), i.e. the ning to 0. i <b>ster</b> 29:16	0	Divide 1	he value he vertica 13:0
0x8001002C	Long	-	by 2 after of Last vertica The last ver counter read VGA Data Bit Name	alculati al positi tical pos ches bef a amou 31:30 Reserv	on. on: iition (in l fore retur int regi	ines), i.e. the ning to 0. i <b>ster</b> 29:16	e last val 15:14 Reserved	Divide 1 ue that Visible	he value he vertica 13:0 screen data
0x8001002C	Long	-	by 2 after of Last vertica The last ver counter read VGA Data Bit Name Read/Write	alculati al positi tical pos ches bef a amou 31:30 Reserv R	on. on: isition (in l fore retur Int regi ed Virtua	ines), i.e. the ning to 0. i <b>ster</b> 29:16 Il screen data R+W	e last val 15:14 Reserved R	Visible	he value he vertica 13:0 screen data R+W
0x8001002C	Long	-	by 2 after of Last vertica The last ver counter read VGA Data Bit Name	alculati al positi tical pos ches bef a amou 31:30 Reserv R	on. on: isition (in l fore retur Int regi ed Virtua	ines), i.e. the ning to 0. i <b>ster</b> 29:16	e last val 15:14 Reserved	Visible	he value he vertica 13:0 screen data
		Re+Ŵr	by 2 after of Last vertica The last ver counter read VGA Data Bit Name Read/Write Reset value Virtual scree The number to be skippe longword re whole 16-bit Visible scree The number always 0, so the nearest	alculati al positi tical positi tical positi tical positi tical positi a amou a amou a amou a amou a amou a amou a amou a a a a a a a a a a a a a a a a a a a	on. on: fore retur int regi ed Virtua o 0b000 i: s on a vir ch row). s always a: s on a vir s on a vir ch row). s always	ines), i.e. the ning to 0. ister 29:16 al screen data R+W 00000000000 ctual screen Note that bit 0, so only events sible screen tes are possible extra rea	e last val 15:14 Reserved R 0b00 row (the 0 (at pos- ven bytes row. Not	Visible visible obout oboooooooooooooooooooooooooooooooo	he value he vertica 13:0 screen data R+W 0000000000 lata + data in the ssible, i.e. ts 3:0 are nd up to
0x8001002C	Long	-	by 2 after of Last vertica The last ver counter read VGA Data Bit Name Read/Write Reset value Virtual scree The number to be skippe longword re whole 16-bi Visible scree The number always 0, so	alculati al positi tical positi tical positi tical positi a amou a ana a amou a ana a amou a ana a amou a ana a amou a ana a amou a ana a amou a ana a ana a a amou a ana a ana a a amou a ana a ana a ana a ana a ana a ana a ana a amou a ana a ana a ana a ana a ana a amou a ana a ana a ana a amou a ana a ana a ana a ana a ana a ana a amou a ana a ana a a ana a ana a a ana a a ana a a a	on. on: ition (in l fore retur int regi ed Virtua o оьооо co оьооо co оьооо co оьооо co оьооо co оьооо co оьооо co оьооо co oьооо co oьооос co oьоо co oьооо co oьооос co oьоо co oьоос co oьоос co oьоос co oьоос co oьоос co oьоос co oьо co оьо со со со со со со со со со со со со со	ines), i.e. the ning to 0. ister 29:16 Il screen data R+W 00000000000 tual screen Note that bit 0, so only events sible screen tes are poss he extra rea ngs	e last val 15:14 Reserved R 0b00 row (the 0 (at pos- ven bytes row. Not sible. Alw d data wi	Visible visible o oboooo visible o sition 16 s are po e that bi rays rou Il be dis	he value he vertica 13:0 screen data R+W 0000000000 data + data in the ssible, i.e. ts 3:0 are nd up to carded.
		Re+Ŵr	by 2 after of Last vertica The last ver counter read VGA Data Bit Name Read/Write Reset value Virtual scree The number longword re whole 16-bi Visible scree The number always 0, so the nearest VGA Vide	alculati al positi tical positi tical positi tical positi tical positi a amou a amou a amou Reserv R a 0b00 een data r of bytes d on ea egister) is t words. een data r of bytes b only ev 16 bytes eo mod	on. on: ition (in l fore retur int regi d Virtua o 0b000 i: s on a via ch row). s always a: s on a via yen 16 by s, since t le setti 31:6	ines), i.e. the ning to 0. ister 29:16 Il screen data R+W 00000000000 rtual screen Note that bit 0, so only events ible screen tes are possible screen tes are possible screen tes are possible screen	e last val 15:14 Reserved R 0b00 row (the 0 (at pos- ven bytes row. Not sible. Alw d data wi	Visible visible oboooo visible oboooo visible castion 16 are po e that bi ays rou Il be dis	he value he vertica 13:0 screen data R+W 0000000000 lata + data in the ssible, i.e. ts 3:0 are nd up to carded. 2:0
		Re+Ŵr	by 2 after of Last vertica The last ver counter read VGA Data Bit Name Read/Write Reset value Virtual scree The number to be skippe longword re whole 16-bi Visible scree The number always 0, so	alculati al positi tical positi tical positi tical positi tical positi a amou a amou a amou Reserv R a 0b00 een data r of bytes d on ea egister) is t words. een data r of bytes b only ev 16 bytes eo mod	on. on: ition (in l fore retur int regi ed Virtua o оьооо co оьооо co оьооо co оьооо co оьооо co оьооо co оьооо co оьооо co oьооо co oьооос co oьоо co oьооо co oьооос co oьоо co oьоос co oьоос co oьоос co oьоос co oьоос co oьоос co oьо co оьо со со со со со со со со со со со со со	ines), i.e. the ning to 0. ister 29:16 Il screen data R+W 00000000000 tual screen Note that bit 0, so only events sible screen tes are poss he extra rea ngs	e last val 15:14 Reserved R 0b00 row (the 0 (at pos- ven bytes row. Not sible. Alw d data wi	Visible visible o oboooo visible o sition 16 s are po e that bi rays rou Il be dis	he value he vertica 13:0 screen data R+W 0000000000 lata + data in the ssible, i.e. ts 3:0 are nd up to carded. 2:0 Video
		Re+Ŵr	by 2 after of Last vertica The last ver counter read VGA Data Bit Name Read/Write Reset value Virtual scree The number longword re whole 16-bi Visible scree The number always 0, so the nearest VGA Vide	alculati al positi tical positi tical positi tical positi a amou a ana a amou a amou a amou a amou a ana a amou a amou a ana a amou a ana a amou a ana a amou a ana a amou a ana a amou a ana a a amou a ana a amou a ana a amou a	on. on: ition (in l fore retur int regi d Virtua o 0b000 i: s on a via ch row). s always a: s on a via yen 16 by s, since t le setti 31:6	ines), i.e. the ning to 0. ister 29:16 Il screen data R+W 00000000000 tual screen Note that bit 0, so only events isible screen events are possible screen tes are possible sc	e last val 15:14 Reserved R 0b00 row (the 0 (at pos- ven bytes row. Not sible. Alw d data wi 4 Double pixel	Visible visible obootoon visible obootoono visible obootoono visible obootoono visible obootoono visible obootoono visible obootoono visible obootoono visible obootoono visible obootoono visible obootoono visib	he value he vertica 13:0 screen data R+W 0000000000 lata + data in the ssible, i.e. ts 3:0 are nd up to carded. 2:0 Video

			Bits 2:0	Video	o mod	e		
			0b000	1-bit l	oitplan	e (Falcon030	compatib	le)
			0b001	2-bit l	oitplan	e (Falcon030	compatib	le)
			0b010	4-bit l	oitplan	e (Falcon030	compatib	le)
			0b011	8-bit l	oitplan	e (Falcon030	compatib	le)
			0b100	8-bit o	chunky	V		
			0b101		,	; color (Falcon0	30 compa	tible)
			0b110	reserv	-			,
			0b111			olor (24-bit RC	GB + alph	a bvte)
							•	
0x80010034	Long	Long	horisontally. T timing (640x4 Line doublin Set to '1' to m	ouble the This is ne 80). <b>g:</b> I resolution h VGA tir	eded t n visibl on. Th ning (6	le line be drav is is needed t	vide resolu vn twice, i	ition with VGA .e. halve the
		Re+Wr						
			Bit	31:27			26:1	0
			Name Read/Write	Reserve	ed	Vic	leo address R+W	0 R
			Reset value	0b0000	0	060000000000000000000000000000000000000		
			Screen addre	When rea	ading f	ut bit 0 is alwa this add 0xA0	ays 0, so a	n odd adress is
0x80010038	Long	Long Re+Wr	DVI Horiso	ontal da	ta be	egin/end re	gister	
			Bit	31:27		26:16	15:11	10:0
			Name	Reserved	Hor	. data begin	Reserved	Hor. data end
			Read/Write	R		R+W	R	R+W
			Reset value	0b00000	0b00	000000000	0b00000	0600000000000000
			Counted in vi calculation. Horisontal d Horisontal po	sition on deo clock ata end: sition on	a scar c pulse a scar	nline where th	vide the v e data wir	alue by 2 after
0x8001003C	Long	Long Re+Wr	DVI Horiso	ontal sy	nc re	egister		
			Bit	31 3	0:27	26:16	15:11	10:0
	1	1						
			Name P	olarity Re	served	Hor. sync begin	Reserved	Hor. sync end
				olarity Re	served R	Hor. sync begin R+W	Reserved	R+W

			<ul> <li>Polarity: Select sync polarity. '1' means sync pulse is active high.</li> <li>Horisontal sync begin: Horisontal position on a scanline where the hsync pulse begins. Counted in video clock pulses (pixels). Divide the value by 2 after calculation. Horisontal sync end: Horisontal position on a scanline where the hsync pulse ends. Counted in video clock pulses (pixels). Divide the value by 2 after calculation.</li> <li>DVI Vertical data begin/end register</li> </ul>								
0x80010040	Long	Long Re+Wr	DVI Vertio	cal dat	a beç	gin/end regi	ster				
			Bit	31:	27	26:16	15:11	10:0			
			Name	Rese	ved	Vert data begin	Reserved	Vert data end			
			Read/Write	R		R+W	R	R+W			
			Reset value	0b00	000	0b00000000000	0b00000	060000000000000000000000000000000000000			
0x80010044	Long	Long Re+Wr	Vertical data begin: Vertical position (in scanlines) where the data window begins. Vertical data end: Vertical position (in scanlines) where the data window ends. DVI Vertical sync register								
			Bit	31	30:27	26:16	15:1	1 10:0			
			Name	Polarity	Reserve						
			Read/Write	R+W	R	R+W	R	R+W			
			Reset value	1	06000	Ороооооооо	00 0b000	00 0b000000000			
			Vertical syn Vertical pos Vertical syn	nc begi ition (in nc end:	n: scanlir	eans sync pulse nes) where the nes) where the	vsync pu	lse begins.			
0x80010048	Long	Long Re+Wr	DVI Last	horisc	ontal/v	vertical pos	ition re	gister			
			Bit	31:2	7	26:16	15:11	10:0			
			Name	Reser	ved	Last hor. pos.	Reserved	Last vertical pos.			
			Read/Write	R		R+W	R	R+W			
			Reset value	0b000	000 0	b0000000000	0b00000	060000000000000000000000000000000000000			
			horisontal c by 2 after c Last vertica The last ver	isontal ounter r alculat al posit tical posit	position eaches i <b>on.</b> ion: sition (i	n (in pixels), i.e s before returni	ng to 0. <b>E</b>	value that the <b>Divide the value</b> le that the vertical			
0x8001004C	Long	Long	DVI Data	amou	nt reg	jister					
		Re+Wr									
		Re+vvr	Bit	31:3	0	29:16	15:14	13:0			

			Read/Write	R	R	+W	R	R+	W	
			Reset value	e 0b00	0600000	000000000	0b00	0b00000	00000000	
			Virtual scr The numbe to be skippe longword re whole 16-b Visible scr The numbe always 0, s the nearest	er of bytes ed on ea egister) is it words. reen data er of bytes o only ev	s on a virtua ch row). No always 0, : s on a visib en 16 byte	te that bit so only ev le screen s are poss	0 (at pos ven bytes row. Note sible. Alwa	ition 16 ir are poss that bits ays round	the ible, i.e. 3:0 are l up to	
0x80010050	Long	Long Re+Wr	DVI Vide	o mode	settings	5				
			Bit	3	1:6	5	4	3	2:0	
			Name	Re	served	Line doubling	Double pixel width	ST comp.	Video mode	
			Read/Write		R	R+W	R+W	R+W	R+W	
			Reset value		0000000000 000000	0b0	0b0	0b0	0b000	
			Bits 2:0	Vid	eo mode					
			0b000	1-b	it bitplane F	alcon030	mode			
			0b001	2-b	it bitplane F	alcon030	mode			
			0b010	4-b	it bitplane F	alcon030	mode			
			0b011	8-b	it bitplane F	alcon030	mode			
			0b100	8-b	it chunky					
			0b101	16-	bit highcold	or Falcon0	30 mode			
			0b110	res	erved					
			0b111	32-	bit truecolo	r (24-bit F	GB + alp	ha byte)		
0.0001000			ST compaties Set to '1' to Double pix Set to '1' to horisontally timing (640 Line doubles Set to '1' to visible vertion resolution v	turn on S <b>cel width</b> double t 2. This is x480). <b>ling:</b> make ea cal resolu vith VGA	ST compati ne pixel wid needed to g ch visible l ution. This i timing (640	ine be dra s needed	lve the ar wide reso wn twice	mount of lution wit	pixels h VGA	
0x80010054	Long	Long Re+Wr								
			Bit	31			30:16			
				G enable R+W		N	lagic key W			
			Write			0/000				
			Reset value	0		%0000	000000000000000000000000000000000000000	00		
			Bit			15:4				
			Name			Reserved				

			Read/ Write			R	
			Reset value		%0000	0000000	
			Bit	3	2	1	0
			Name	JTAG TCK	JTAG TMS	JTAG TDI	JTAG TDO
			Read/ Write	R+W	R+W	R+W	R
			Reset value	0	1	1	?
0x80010058	Long	Long	modify JTAG 0=JTA 1=JTA memory JTAG When the PR JTAG When going f of the is externa be use the sig JTAG When going f of the is the ext cannot drive th JTAG When going f of the is the ext cannot drive th	the JTAG b enable: G interface G enabled a ries. TDO: read, return OMs to the TDI: written, com from the FP internal JTA al signal bet d to detect a nals. TMS: written, com from the FP internal signal a be used to ne signals. TCK: written, com from the FP internal signal a be used to ne signals.	i.e. every write to its must have this disabled and JTAC and FPGA is drivin s the level of the C FPGA. trols the output lev GA to the PROMs G TDI signal in the ween the FPGA a a possible externa trols the output lev GA to the PROMs G TMS signal in the between the FPG detect a possible trols the output lev GA to the PROMs G TCK signal in the between the FPG detect a possible	value at bits 30 G pins in high ir g JTAG pins to ITAG-TDO sign vel of the JTAG . When read, re e FPGA and no nd the PROMs I JTAG master vel of the JTAG . When read, re the FPGA and n GA and the PRC external JTAG when read, re the FPGA and n GA and the PRC external JTAG	0-16. mpedance. wards PROM al going from -TDI signal eturns the level t the level of the . So this cannot trying to drive -TMS signal eturns the level of the level of DMs. So this master trying to -TCK signal eturns the level of the level of DMs. So this
0x80010058	Long	Long Re+Wr	Supe		ource1 addres	s register	
			Bit	31:27		26:0	
			Name Read/	Reserved R		Source address 1	
			Write				
			Reset value	0b00000	0600000	000000000000000000000000000000000000000	000000
			The ac	Iress of the	main data source,	addressing by	tes.
0x8001005C	Long	Long Re+Wr	Supe	rBlitter so	ource2 addres	s register	
			Bit	31:27		26:0	
			Name	Reserved	5	Source address 2	

			Read/ Write	R		R+W	
			Reset value	0b00000		060000000000000000000000000000000000000	000000
			source	is only use	ed w	ondary data source, addressin hen doing some kind of arithn src2 data before writing it to th	netic/logic
0x80010060	Long	Long Re+Wr	Supe	rBlitter d	lest	ination address registe	er.
			Bit	31:27		26:0	
			Name	Reserved		Destination address	
			Read/ Write	R		R+W	
			Reset value	0b00000		060000000000000000000000000000000000000	000000
			The ad	lress of the	des	tination, addressing bytes.	
0x80010064	Long	Long Re+Wr	Supe	rBlitter li	ine	byte count register	
			Bit	31:24		23:11	10:0
			Name	Alpha value mode 0b01		Reserved	Line byte count
			Read/ Write	R		R	R+W
			Reset value	0600000	00	060000000000000	060000000000000000000000000000000000000
			The an minus <b>Alpha</b> This 8- each p	<ol> <li>To copy</li> <li>value for r</li> <li>bit alpha value</li> </ol>	1 by <b>nod</b> alue entire	that are to be copied in a horiz yte, write 0 here. I <b>e 0b0111:</b> is used for the 0b0111 blitter e Src1 block uses the same a	mode, where
0x80010068	Long	Long Re+Wr	Supe	rBlitter s	oui	rce1 line offset register	
			Bit	31:27		26:0	
			Name	Reserved		Line offset	
			Read/ Write	R		R+W	
			Reset value	0b00000		060000000000000000000000000000000000000	000000
			after a line sta	line has be art address.	en o . Neg	that are to be added to the line copied, in source1, in order to gative amounts (address decr bers starting with '1' here (in l	reach the next ements) can be
0x8001006C	Long	Long Re+Wr	Supe	rBlitter s	oui	rce2 line offset register	
			Bit	31:27		26:0	
			Name	Reserved		Line offset	
			Read/ Write	R		R+W	

			Reset value	0b0000	0	0b0	000000000	00000000	0000000	0000			
			The amount of bytes that are to be added to the line start adress after a line has been copied, in source2, in order to reach the next line start address. Negative amounts (address decrements) can be realised by using numbers starting with '1' here (in bit 26).								e next		
0x80010070	Long	Long Re+Wr SuperBlitter destination line offset register						r					
			Bit	Bit 31:27 26:0									
			Name	Reserve	d		l	_ine offset	t				
			Read/ Write	R				R+W					
			Reset value	0b0000	0	ObC	00000000	00000000	0000000	0000			
0x80010074	Long	Long	after a next lir can be	line has ne start a realised	been co address. d by usir	opied, in Negativ ng numb	destinat e amour ers start	dded to the line start adress nation, in order to reach the ounts (address decrements) arting with '1' here (in bit 26).					
0,000,001,4	Long	Re+Wr	SuperBlitter address mask and number of lines register										
			Bit	31:	24	23:	16	15:12		11:0			
			Name	Src1 a count r		Src2 ac count n		Reserved	Nui	nber of	lines		
			Read/ Write	R+	W	R+	w	R		R+W			
			Reset0b00000000b00000000b000value0b00000000b00000000b0000000					0b0000	060000000000000000000000000000000000000				
		Src1 adress count mask: A mask to apply to the source1 address counter while incr it during the write phase. The value set will make the adre at that value. Only 2^n values are possible: 0,1,2,4,8128 that we're counting 64-bit words here, not bytes, since the works with 64-bit words internally. Also note that it is only t counter, that is added to the src1 base address, that is affe this mask, not the src1 base address itself. Setting the ma will turn off masking of the address counter (but it can only 255 anyway).							adress .128. I the bl nly the affec mask	wrap Note litter e ted by a to 0			
			<b>Src2 address count mask:</b> The same as the src1 address mask above, but for src2.						c2.				
				<b>er of lin</b> nount of		tal lines	to do.						
0x80010078	Long	Long Re+Wr	SuperBlitter control and status register										
			Bit	31:24	23:16	15:8	7	6	5	4:1	0		
			Name	Replace Red	Replace Green	Replace Blue	Replace Enable	Done INT flag	INT enable	Blit mode	Busy (read) Start (write)		
			Read/ Write	R+W	R+W	R+W	R+W	R+W	R+W	R+W	R+W		
			Reset	0b0000	0b0000	0b0000	0b0	0b0	0b0	0b00	0		

value	0000	0000	0000				00	(read),
							00	0 (write)
When the Su registe	uperBli ers are	usy bit rea tter again properly is busy po	. But ma set up fi	ke sure th rst! While	hat the o this bit	other Su is set to	iperB ) '1' th	litter
		es, the bits	s are not e			kpected o	rder)	:
Coc				Blit m	node			
00d0		est = src1						
0b00		eserved						
0b01 0b01		eserved						
0b01		eserved						
0b10		eserved						
0b10		eserved						
0b11		eserved eserved						
0000	01 de Ea	eserved est = src1 ich <b>byte</b> of s t 0. For 8-bi r 16-bit spri	src1 is writt t chunky m	en to dest if ode: src1=s	f the corre src2=sprit	esponding e data	byte c	of src2 is
0000	11 de 32	est = src1 -bit pixel alp aly the alpha	* <i>src1.al</i> ha blendin	<b>pha + src</b> g. Each pix	2 * <b>(25</b> ) el is R,G,	6-src1.a		
0b01	Ea	est = src1 ich 16bit wo e green chai	rd of src1 i	s written to				s bit 0 of
0b01	32 R,9	est = src1 src2 -bit pixel alp G,B,A. 8 bits gister at 0x8	* <b>(256 -</b> ha blendin s per chanr	src1.alph g with globa	a <sup>*</sup> alph al alpha e	n <b>a_reg)</b> effect too. E	Each p nes fro	pixel is om the
0b10	01 <b>R</b> e	eserved						
0b10	11 <b>R</b> e	eserved						
0b11	01 <b>R</b>	eserved						
0b11	11 <b>R</b>	eserved						
Writin reque set to flag. I (addre	g INT e st whe 1. You Make s ess 0x3	ble & Done INT flag NT enable to 1 makes the blitter generate an interrupt when it completes a blitting job, and Done INT flag will be You must clear it in your handler by writing 0 to Done INT ke sure you put your ISR pointer in vector number 0xC6 (0x318) before starting a blitter job with interrupts enabled. v 6 firmware the Done INT flag can be written to '1' to make r immediately generate a Done interrupt, if it was idle (if r was busy with an operation nothing will happen). ble must also be set for this to work.						will be ne INT 0xC6 nabled.
the bli the bli	tter im							
This e	nables modes	able and s replacing s (0b0011 ace Red,	g of the F and 0b0	RGB part 111) with	of sour	ce1 in 32		

0x8001007C	Long	Long Re	Super	Videl version re	gister			
			Bit		31:10	9:0		
			Name	R	eserved	Revision		
			Read/ Write		R	R		
			Reset value	060000000	000000000000000000000000000000000000000	?		
0x80010080	Long	Long Re+Wr		on: I revision of SV firm\ Blitter register I				
			Bit	31:2	1	0		
			Name	FIFO port bits 31:2	FIFO port bit 1 (write) FIFO full flag (read)	FIFO port bit 0 (write) FIFO empty flag (read)		
			Read/ Write	W	R+W	R+W		
			Reset value         -         Ob0         Ob0					
			FIFO per Write to Starting 0x8001 order. V is idle, r the regi started, FIFO er Is '1' wh FIFO fu	this 32bit port to qu a blitter operation re 0058 and going up to Vhen the FIFO holds nine longwords will b sters at 0x80010058 if the control register <b>mpty flag:</b> nen the blitter FIFO h all flag:	m FW revision 9. eue SuperBlitter reg equires nine register o and including 0x80 at least nine longwo be read out from the 3-0x80010078, and the r holds such settings holds less than 9 long holds 500 or more long	writes, starting at 0010078, in that ords and the blitter FIFO to overwrite he blitter will be s. gwords.		

## Ethernet MAC core registers

Address	Size	Access types	Description			
0x80012000- 0x80012053	84 bytes	Long Re+Wr	Ethernet MAC core control registers			
			See eth_speci.pdf, section 3.			
0x80012400- 0x800127FF	1024 bytes	Long Re+Wr	Ethernet MAC core buffer descriptors			
			See eth_design_document.pdf: section 2.3.7.3, and eth_speci.pdf: section 4.2.2.			
0x80012800- 0x80013FFF	6144 bytes	Long Re+Wr	Ethernet MAC core data buffers			
			3 blocks of 2048 bytes form 4 packet buffers of 1536 bytes each. Note that writing this using other sizes than Long will corrupt data. <i>These buffers are removed from FW v10. The buffers then reside</i> <i>in DDR2 RAM instead.</i>			

## 256 color palette

Address	Size	Access types	Description						
0xFFFF9800	1024 bytes	Byte Word Long	<b>256 color palette</b> Each longword entry looks like this:						
		Re+Wr	Bit	31:24	23:16	15:8	7:0		
			Name	Red	Green	Reserved	Blue		
				Read/Write	R+W	R+W	R	R+W	
			Reset value	0x00	0x00	0x00	0x00		